AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Listing of Claims:

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1. (Currently Amended) An apparatus comprising: ~~A synchroniser for use in~~ a receiver ~~which receives~~ for receiving a signals~~,~~ ; and ~~said~~

a synchroniser including a digital signal processor for processing the signal, wherein said synchroniser is configured to:

provide a digital control signal, said control signal defining a plurality of different levels;

control the level provided by successive ones of said control signals, successive ones of said control signal defining different values;

convert said digital control signal into an analog control signal for controlling a mixing frequency; and

estimate the difference between the levels of successive ones of said analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels.

2. (Canceled)

3. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said providing, said

controlling and said estimating are performed in ~~the~~ a digital domain.

4. (Currently Amended) The ~~synchroniser~~ apparatus of claim 3, wherein said providing, said controlling and said estimating are provided in the digital signal processor.

5. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said providing is performed by a digital corrector.

6. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein a rough correction is provided by said control signal.

7. (Currently Amended) The ~~synchroniser~~ apparatus of claim 6, wherein a rough correction is provided in an analog domain.

8. (Currently Amended) The ~~synchroniser~~ apparatus of claim 6, wherein a finer correction is provided.

9. (Currently Amended) The ~~synchroniser~~ apparatus of claim 8, wherein said finer correction is provided in a digital domain.

10. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said estimating is performed by an estimator configured to determine that the difference between two successive levels has increased if a difference between the upper of said levels and an estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

11. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said estimating is performed by an estimator configured to determine that the difference between two successive levels has increased if a difference between the upper of said levels and an estimated level for an actual signal provides a signal at a higher level than a signal provided

by a difference between a lower of said levels and an estimated level for the actual signal.

12. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said estimating is performed by an estimator configured to determine that an actual signal has changed if a difference between the upper of said levels and an actual signal provides a signal at substantially the same level as a signal provided by a difference between a lower of said levels and the actual signal, said same level being different to a previous level for said actual signal.

13. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said synchroniser is arranged to at least one of acquire and track frequency error.

14. (Currently Amended) The ~~synchroniser~~ apparatus of claim 1, wherein said synchroniser is arranged to at least one of acquire and track timing error.

15. (Currently Amended) The apparatus of claim 1 embodied on a wireless receiver ~~comprising the synchroniser as claimed in claim 1~~.

16. (Canceled)

17. (Currently Amended) The apparatus ~~synchroniser~~ of claim 1, wherein said providing means, said controlling means and said estimating means are in ~~the~~ a digital domain.

18. (Currently Amended) The apparatus ~~synchroniser~~ of claim 7, wherein a finer correction is provided.

19. (Currently Amended) The apparatus ~~receiver~~ of claim 15, further comprising:

an antenna for receiving signals;

a first bandpass filter for filtering out unwanted signals;

a mixer for downconverting received signals to a baseband frequency;

a second bandpass filter for removing unwanted signals falling outside the bandwith of said second bandpass filter;

an analog to digital converter for converting signals received from said second bandpass filter from analog to digital form; and

a digital to analog converter for converting the signals received from said digital signal processor from digital to analog form.

20. (Currently Amended) The apparatus ~~receiver~~ of claim 19, wherein said digital signal processor comprises:

a detector for measuring frequency errors and sending a digital word;

a filter for filtering said digital word output by said detector;

a step size estimator for estimating an actual step size of a frequency change provided by said digital to analog converter and providing said actual step size to analog correction; and

a digital automatic frequency control unit for controlling division of correction between analog and digital parts, performing an accurate correction so that a zero or close to zero error is achieved and compensating for the effect of an analog control for which a step size is estimated while a control word is changed.

21. (Currently Amended) A method comprising: ~~for~~ receiving a signal on a receiver; and

providing synchronization in a the receiver of the received signal, further comprising ~~the steps of~~:

providing a digital control signal, said control signal defining a plurality of different levels;

controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values;

converting the digital control signal into an analog control signal for controlling a mixing frequency; and

estimating the difference between the levels of successive ones of said analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels.

22. (Currently Amended) A computer program product embodied on a computer-readable medium comprising instructions that when executed result in operations for providing synchronization in a receiver, ~~the computer-readable medium being encoded with a computer program, the computer program~~ comprising:

~~program code for~~ providing a digital control signal, said control signal defining a plurality of different levels;

~~program code for~~ controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values;

~~program code for~~ converting the digital control signal into an analog control signal for controlling a mixing frequency; and

~~program code for~~ estimating the difference between the levels of successive ones of said analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels.

23. (Currently Amended) A synchronizer for use in a receiver which receives signals, said synchronizer comprising:

means for providing a digital control signal, said control signal defining a plurality of different levels;

means for controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values;

means for converting said digital control signal into an analog control signal for controlling a mixing frequency; and

means for estimating the difference between the levels of successive ones of said analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels.

24. (New) A synchronizer for use in a receiver comprising:

a digital to analogue convertor; and

a digital signal processor having a detector configured to provide a digital control signal, said control signal defining a plurality of different levels, wherein the level provided by successive ones of said control signals is controlled so that successive ones of said control signal defining different values, wherein said digital to analogue converter is configured to convert for estimating the difference between the levels of successive ones of said analog control signal and send digital signal processor has a step size estimator configured to estimate the differences

between the levels of successive ones of said analog control signal, wherein said differences are used to estimate a step size between the successive analog control signal levels.